Digital Modulation

Modules: Sequence Generator, Digital Utilities, VCO, Multiplier, Dual Analog Switch, Quadrature Utilities, FM Utilities, 100-kHz Channel Filters, 60-kHz LPF, Tuneable LPF, Adder

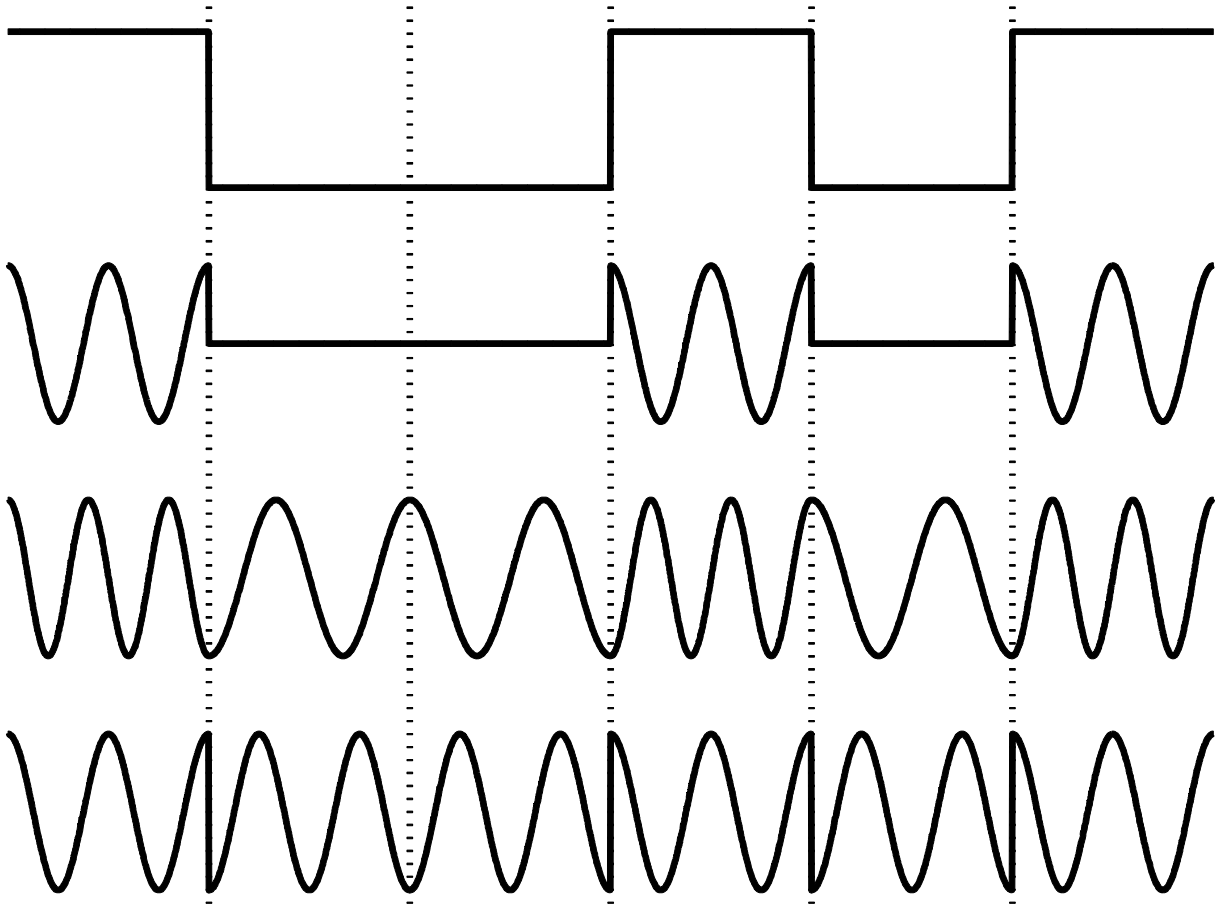
0 Pre-Laboratory Reading

Most new radio communication systems employ digital communication, for which the message, in digital form, is modulated in a discrete manner onto a carrier. The carrier is always analog, as it must be in order to propagate from the transmitter to the receiver.

Digital communication systems can convey analog information, such as voice. At the transmitter, the analog message signal is sampled, and then the samples are quantized. The result of this *analog-to-digital conversion* is that each sample is represented by a word that consists of a set number of bits. Each bit can be represented in a circuit with TTL levels or with bipolar (positive/negative) voltages. The words representing the samples are arranged in proper order, and so the original analog signal can be represented as a stream of TTL or bipolar voltages. An analog carrier conveys a stream of TTL or bipolar voltages by means of digital modulation.

Digital modulation of an analog carrier means that the signal information is impressed upon the carrier using only a discrete number of possible changes. The three most fundamental types of digital modulation are: amplitude-shift keying (ASK), frequency-shift keying (FSK), and phase-shift keying (PSK). More complicated digital modulation schemes are built from these fundamental types.

ASK, FSK and PSK are illustrated below. At the top of this illustration is a bit stream. With ASK the carrier amplitude has, during any given bit interval, one of two values. One of these values can be zero, as shown below. With FSK the carrier frequency, during any given bit interval, has one of two values. With PSK one bit is conveyed at a time by one of two possibilities: the carrier phase is $2\pi f_c t$ (where f_c is the carrier frequency) or the carrier phase is $2\pi f_c t - \pi$. A PSK carrier therefore experiences an abrupt phase change of 180° at every instant when the bit changes (from 0 to 1 or from 1 to 0).

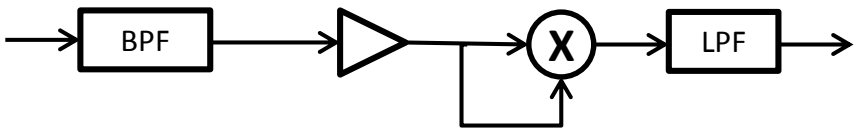


First row	bit stream
Second row	ASK
Third row	FSK
Fourth row	PSK

0.1 ASK

A carrier with ASK can be generated using a switch. An unmodulated sinusoid at the carrier frequency either passes through the switch or is blocked, depending on the current bit.

ASK demodulation can be accomplished with a noncoherent receiver. That is to say, there is no need for a carrier reference at the receiver.



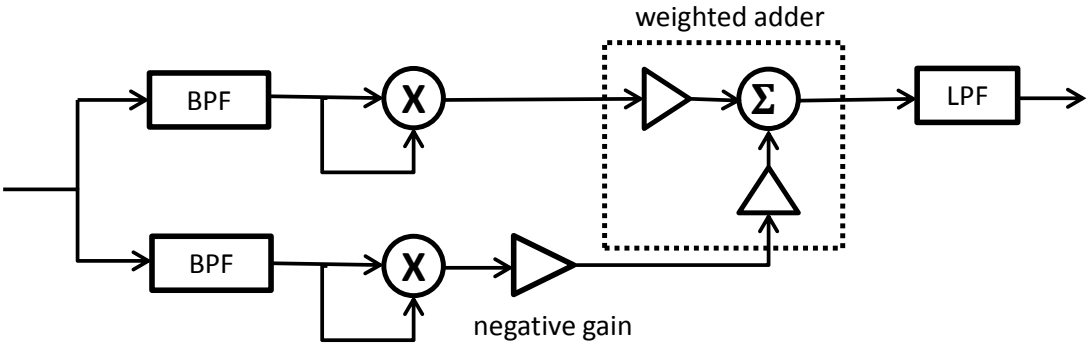
ASK demodulator

The arriving carrier is first subjected to bandpass filtering. This will pass the carrier but block that portion of the noise (and interfering signals) whose spectral content is not near the carrier frequency. The squaring operation produces a DC term and a double-frequency term (when the carrier is present). The lowpass filter will block the double-frequency term. This demodulator will therefore convert a carrier with ASK back into a bit stream (a positive voltage when the carrier is present, and zero when the carrier is absent).

0.2 FSK

A carrier with FSK can be generated with a VCO. A TTL signal at the (data) input to the VCO determines which of two frequencies will be produced at the VCO output.

A carrier with FSK can be demodulated with a noncoherent receiver.



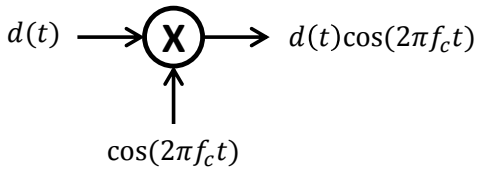
FSK demodulator

The upper branch of this demodulator has a bandpass filter designed to pass one of the two expected frequencies of the arriving carrier (and to block the other). The lower branch plays the reverse role. Each squaring operation creates a DC term and a double-frequency term. The elimination of the double-frequency term from each branch is accomplished with one common lowpass filter at the back end of the demodulator. One branch of the demodulator will experience a net positive gain before the addition, and the other branch will experience negative gain before the addition. The output of this demodulator will therefore be a positive DC voltage in response to one frequency and a negative DC voltage in response to the other.

In this experiment, the (weighted) Adder incorporates negative gain at each input (shown in the above diagram). Therefore, the lower branch with a separate amplifier, having negative gain, will have a net positive gain. A positive DC voltage at the demodulator output is the response to an arriving frequency that passes through the lower bandpass filter. The upper branch has a negative gain (arising in the weighted Adder). A negative DC voltage at the demodulator output is the response to an arriving frequency that passes through the upper bandpass filter.

0.3 PSK

A carrier with PSK can be generated with a multiplier:



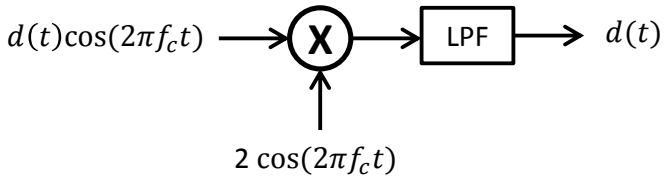
PSK modulator

This can be described in mathematics like this:

$$y(t) = d(t)\cos(2\pi f_c t) \tag{1}$$

where $d(t) = \pm 1$ is the sequence of bipolar voltages representing the data and f_c is the carrier frequency. It should be noted that multiplying a sinusoid by -1 is equivalent to shifting the phase by 180°.

A demodulator for PSK might look like this:



PSK demodulator (synchronous detector)

This assumes that a coherent carrier reference is available in the receiver. This is known as a synchronous detector. In this experiment, a stolen carrier (from the transmitter) will be used.

The output of the multiplier in the synchronous detector is:

$$d(t)\cos(2\pi f_c t) \cdot 2\cos(2\pi f_c t) = d(t) + d(t)\cos(4\pi f_c t)$$

The double-frequency term is blocked by the lowpass filter, leaving only $d(t)$ to pass through to the demodulator output.

When the receiver is in the field, distant from the transmitter, no stolen carrier is available to the receiver. In general, a PSK receiver will employ a type of phase-locked loop, known as a Costas loop, to provide carrier synchronization. This will not be done in this experiment.

1 ASK

The Sequence Generator module will supply a sequence of TTL voltages (representing a stream of bits). On the PCB of this module there is a pair of switches in a dual in-line package (DIP). These switches determine the sequences. Set both switches to the up position. You will use the sequence at the TTL Y output port.

Use a TTL clock with frequency $(100/48)$ kHz to clock the Sequence Generator. You may create this TTL clock by connecting a $(100/12)$-kHz TTL clock (labeled as the 8.3-kHz TTL clock on the Master Signals panel) to the input of a divide-by-4 function on the Digital Utilities module.

Place the TTL Y output from the Sequence Generator on Channel A. Place the (TTL) sync output of the Sequence Generator on Channel B. Use this same sync output as the trigger source. (A positive trigger level is needed for a TTL trigger source.) The sequence from the TTL Y output is periodic. The sync TTL signal has the same period and therefore permits a stable oscilloscope display. You should observe a stable display of a sequence of binary-valued voltages.

Channel A: TTL Y output of Sequence Generator
Channel B: TTL synch output of Sequence Generator

Generate an ASK carrier using a Dual Analog Switch. Connect a 100-kHz sinusoid to one of the analog inputs of the switch. To the corresponding TTL control input, connect the TTL Y output of the Sequence Generator. A high level (approximately 5 V) on the TTL control signal allows the 100-kHz sinusoid to pass to the output of the Dual Analog Switch. A low level (approximately 0 V) on the TTL control signal blocks the 100-kHz sinusoid.

With the TTL Y output of the Sequence Generator still connected to Channel A, connect Switch output to Channel B. Use the TTL synch signal from the Sequence Generator as the external trigger. You should be able to stabilize both displays (while in continuous capture mode). Both the $(100/48)$ kHz clock (setting the bit rate) and the 100-kHz carrier have frequencies that are integer multiples of the TTL synch frequency.

Channel A: TTL Y output of Sequence Generator
Channel B: Dual Analog Switch output

Observe the spectrum of the ASK carrier.

Channel B: Dual Analog Switch output

The spectrum is more complicated than a single line at 100 kHz since the modulated carrier is not a pure sinusoid, but rather a sinusoid that is being turned on and off.

Construct an ASK demodulator. Connect the ASK carrier to the input of the 100-kHz Channel Filters module, setting the switch to position 3. This is a bandpass filter centered at 100 kHz. Place the bandpass filter output on the input of a Buffer Amplifier and the output of the amplifier on both inputs of a multiplier. The output of the multiplier (used here as a square-law device) should be placed at the input of the 60-kHz LPF.

Place a copy of the Sequence Generator's TTL Y output on Channel A, and connect the BPF output (the output of the filter in the 100-kHz Channel Filters module) to Channel B. Use the TTL synch signal as an external trigger. Adjust the attenuation (provided by the Buffer Amplifier) so that the output of the Buffer Amplifier has a peak value of approximately 1 V.


Channel A: TTL Y output of Sequence Generator
Channel B: BPF output

On Channel B, replace the BPF output with the Multiplier output. Use the TTL synch signal as an external trigger.


Channel A: TTL Y output of Sequence Generator
Channel B: Multiplier output

When the TTL bit is high, the multiplier output should be the sum of a DC term and a double-frequency term. Measure the frequency of that double-frequency term using vertical rulers. It should be 200 kHz.

Observe the spectrum of the multiplier output.


Channel B: Multiplier output

You should see DC and 200-kHz components. But the spectrum will be complicated by the switching action of the modulator.

Place a copy of the Sequence Generator's TTL Y output (the TTL bit stream) on Channel A, and connect the 60-kHz LPF output to Channel B. Use the TTL synch signal as an external trigger.


Channel A: TTL Y output of Sequence Generator
Channel B: demodulator output (the output of the 60-kHz LPF)

You should find that this demodulator recovers the original TTL bit stream (with amplitude scaling and some delay).

2 FSK

As above, use the Sequence Generator to produce a TTL bit stream. However, for the FSK demonstration the bit rate will be (100/96) kHz, rather than (100/48) kHz. The appropriate TTL clock can be created from the (100/12)-kHz TTL clock using a divide-by-4 and a divide-by-2 on the Digital Utilities module. Apply the (100/96)-kHz TTL clock that you have generated to the TTL clock input of the Sequence Generator.

Connect the TTL Y output of the Sequence Generator to Channel A. Use the sync output as the trigger source. You will be using the TTL Y output as the TTL bit stream for the FSK demonstration.

 Channel A: TTL Y output of Sequence Generator

A VCO is used to generate a carrier with FSK. Make sure the switch on the VCO module's PCB is set to "FSK". Set the toggle switch on the front panel of the VCO module to "HI". You will want to place the VCO module into the TIMS instrument frame in such a way that there are at least two open slots to the left of the VCO module. There are two dials on the VCO PCB that you will need to adjust while the VCO is in place.

Connect the TTL bit stream to the TTL data input port of the VCO. In this experiment you will *not* use the analog input port of the VCO. When the VCO module is in the FSK mode, the frequency tuning and gain knobs on the front panel have no effect. You will, however, use the analog output port of the VCO. In summary, when using the VCO module to create an FSK signal, you will use the TTL data input port to convey one of two discrete levels, and you will use the analog output port (since, as always, the modulator output should be analog).

Connect the VCO output to Channel B. Observe the spectrum of the VCO output.

 Channel B: VCO output

You should see two strong peaks in the spectrum. These peaks correspond to the two signaling frequencies. Adjust the two dials on the VCO module's PCB until one peak occurs at approximately 33.3 kHz and the other at approximately 100 kHz.

Place a copy of the TTL bit stream (the Sequence Generator's TTL Y output) on Channel A, and connect the VCO output to Channel B. Use the TTL synch signal as an external trigger.

 Channel A: TTL Y output of Sequence Generator
Channel B: VCO output

Construct an FSK demodulator. Connect the FSK carrier to the inputs of two bandpass filters, one with a center frequency of 100 kHz and the other with a center frequency of 33.3 kHz. The 100-kHz bandpass filter is available on the 100-kHz Channel Filters module (with switch set to position 3). The 33.3-kHz bandpass filter is available on the FM Utilities module. Place the output of the 100-kHz bandpass filter on both inputs of a multiplier, creating a square-law device. Place the output of the 33.3-kHz bandpass filter on both inputs of a second multiplier. You can use the two multipliers on a Quadrature Utilities module. For the 33.3-kHz channel, place the output of the multiplier (used as a square-law device) on the input of a Buffer Amplifier. Place the output of this amplifier and the output of the 100-kHz channel multiplier on the inputs of the (weighted) Adder. Place the Adder output on the input of a Tuneable LPF.

The 33.3-kHz channel of the demodulator experiences a net positive gain since the negative gains of the Buffer Amplifier and the (weighted) Adder cancel. The 100-kHz channel experiences a negative gain (arising in the weighted Adder).

A copy of the TTL bit stream should still be connected to Channel A. Place a copy of the output of the 100-kHz BPF on Channel B. Use the TTL synch signal as an external trigger.


Channel A: TTL Y output of Sequence Generator
Channel B: output of 100-kHz BPF

View the output of the 100-kHz bandpass filter on the spectrum analyzer.


Channel B: output of 100-kHz BPF

On Channel B, replace the output of the 100-kHz BPF with the output of the 33.3-kHz BPF.


Channel A: TTL Y output of Sequence Generator
Channel B: output of 33.3-kHz BPF

View the output of the 33.3-kHz bandpass filter on the spectrum analyzer.


Channel B: output of 33.3-kHz BPF

On Channel B, replace the output of the 33.3-kHz BPF with the output of the 100-kHz channel multiplier (which is being used as a square-law device).


Channel A: TTL Y output of Sequence Generator
Channel B: output of 100-kHz channel multiplier

You should observe that, for some bit intervals, a DC term plus a double-frequency term are present. Measure the frequency of that double-frequency term using vertical rulers.

View the output of the 100-kHz channel multiplier on the spectrum analyzer.


Channel B: output of 100-kHz channel multiplier

On Channel B, replace the output of the 100-kHz BPF with the output of the 33.3-kHz channel multiplier.


Channel A: TTL Y output of Sequence Generator
Channel B: output of 33.3-kHz channel multiplier

You should observe that, for some bit intervals, a DC term plus a double-frequency term are present. Measure the frequency of that double-frequency term using vertical rulers.

View the output of the 33.3-kHz channel multiplier on the spectrum analyzer.


Channel B: output of 33.3-kHz channel multiplier

Adjust the bandwidth of the Tuneable LPF to approximately 26 kHz. (The Tuneable LPF's clock output has a frequency equal to 100 times the bandwidth.) A copy of the TTL bit stream should still be connected to Channel A. Connect the output of the Tuneable LPF to Channel B. Use the TTL synch signal as an external trigger. Adjust the gains of the (weighted) Adder and the gain of the Buffer Amplifier (in the 33.3-kHz channel) until the output of the demodulator is ± 2 V. This represents a successful demodulation of the original bit stream.


Channel A: TTL Y output of Sequence Generator
Channel B: output of demodulator (output of the Tuneable LPF)

3 PSK

You will use a bit rate of (100/48) kHz for this demonstration. Create a $(100/48)$-kHz TTL clock from the $(100/12)$-kHz TTL clock and a divide-by-4 (Digital Utilities). Place the $(100/48)$-kHz TTL clock on the TTL clock input of the Sequence Generator.

In this demonstration, you will use a stream of bipolar voltages, rather than a stream of TTL levels, to represent the bit stream. You will get the bipolar stream from the *analog* Y output of the Sequence Generator. Connect the analog Y output of the Sequence Generator to Channel A. Use the sync output as the trigger source.


Channel A: analog Y output of Sequence Generator

Create a PSK carrier by connecting the analog Y output of the Sequence Generator to one input of the Multiplier and a 100-kHz sinusoid (Master Signals) to the other input. A copy of the Sequence Generator's analog Y output should still be on Channel A. Connect the modulator (Multiplier) output on Channel B. Use the sync output of the Sequence Generator as the trigger source.

Channel A: analog Y output of Sequence Generator
Channel B: output of modulator

Consider using the zoom function of the oscilloscope to zoom in on a data transition. This modulation scheme is also called binary phase-shift keying (BPSK) to emphasize the fact that there are two possible phase states in any given bit interval.

View the modulator output on the spectrum analyzer.

Channel B: output of modulator

You should note that there is no residual carrier.

Build a synchronous detector using a stolen (100-kHz) carrier. Connect the PSK carrier to the input of a multiplier (Quadrature Utilities). Connect the stolen carrier, serving in the place of a local oscillator, to the other input of the multiplier. Connect the output of the multiplier to the input of a Tuneable LPF. Adjust the bandwidth of the Tuneable LPF to approximately 26 kHz.

A copy of the Sequence Generator's analog Y output should still be on Channel A. Connect the synchronous detector output on Channel B. Use the sync output of the Sequence Generator as the trigger source.

Channel A: analog Y output of Sequence Generator
Channel B: output of synchronous detector (stolen carrier)

You should find that the original bit stream has been recovered.

You will now use a VCO to generate a local oscillator for the demodulator, replacing the stolen carrier. Make sure the switch on the VCO module's PCB is set to "VCO" and set the toggle switch on the front panel to "HI". Disconnect the stolen carrier from the demodulator and replace that stolen carrier with the VCO output. Place a copy of the VCO output on the Frequency Counter, and adjust the VCO frequency to approximately 100 kHz.

With the VCO as local oscillator, view the demodulator output on the oscilloscope while also viewing the original bipolar voltage stream. You will find that the display is unstable. This is because the VCO frequency, while approximately 100 kHz, is not coherently related to the

frequencies generated by the crystal oscillator in the Master Signals panel. Therefore, the VCO frequency is not coherently related to the TTL synch frequency from the Sequence Generator.

Try to tune the VCO frequency as close to 100 kHz as possible. (It will drift because the VCO is not a very frequency-stable oscillator. Even if you get very close to 100 kHz, the VCO frequency may not stay there for long.) If you can get the VCO close enough to 100 kHz, you will observe the following. The original bipolar voltage stream may appear at the demodulator output, but the amplitude of this output varies. The amplitude will probably go through zero; and on the other side of zero amplitude, the bits are upside down. This indicates that the local oscillator's frequency is almost right for the demodulation, but its phase drifts.

Channel A: analog Y output of Sequence Generator
Channel B: output of synchronous detector (VCO as local oscillator)

This is a stark demonstration of the need for getting both the phase and frequency of the local oscillator right whenever synchronous detection is used. When a receiver is in the field, remote from the transmitter, so that no stolen carrier is available, it is necessary to lock the phase (and therefore also the frequency) of the local oscillator to that of the arriving carrier. For binary phase-shift keying, this is accomplished with a kind of phase-locked loop called a Costas loop.